| Sundance Multiprocessor Technology Limited<br>**Design Specification** | Form : QCF51<br>Dated : 20th May 1999<br>Revision : 1<br>Approved : Mark Ainsworth |
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| | |
|---|---|
| **Unit / Module Name:** | |
| **Unit / Module Number:** | Sundance Digital Bus Interface |
| **Used On:** | |
| **Document Issue:** | |
| **Date:** | 20/06/00 |

## Outline Description

The Sundance Digital Bus (SDB) was developed as a mean to allow data to be transmitted or received at data rates in excess of the current communication ports 20Mbytes/second.

The ‘C4x Protocol defines Byte-wide links which can theoretically transmit at 20Mbytes/second asynchronously between TIMs. The Sundance data bus uses 16-bits data wide links designed to transmit synchronously at over 200M Bytes/Second.

Each high speed Sundance Digital Bus (SDB) Interface can transfer 16-Bit data, to and from the TIM, at such a transfer rate.

It can be adapted to use two connectors to send a 32-bit data every clock cycle at 100 MHz reaching 400M Bytes/Second.

The SDB Interface transfers 32-bit words in two clock cycles and store two 16-bit data received into a 32-bit word FIFO ready to be used.

Data rates of 200Mbytes/second through a connector have been achieved using a ground interlaced signal cable.

The transmission can be fully bi-directional.

Many of Sundance TIM modules are being designed with this interface.

APPROVED (Managing Director) DATE

APPROVED (Technical Director) DATE

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## Revision History

| Date | Changes Made | Issue | Initials |
|---|---|---|---|
| **12/10/99** | **Initial release** | **1.0** | **J.V.** |
| **18/10/99** | **Protocol extension** | **1.1** | **J.V.** |
| **22/10/99** | **Size and performance added**<br>**LVDS extension detailed** | **1.2** | **J.V.** |
| **04/11/99** | **Voltage Specification** | **1.3** | **J.V.** |
| **20/06/00** | **WEN polarity inverted; now active Low for compatibility with FIFOs and other modules.** | **2.0** | **J.V.** |
| **20/02/01** | **Text corrected page 6.**<br>**Did not match drawing** | **2.1** | **J.V.** |

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# 1. Transmission protocol

A 16-bit data is transmitted at each clock cycle when WEN is Low. (The standard has been modified to allow direct interfacing with FIFO devices and other processor).

On the transmission side the data and the enable signals are set on the bus at the rising edge of the clock and so on the reception side a valid data can be sampled on the rising edge of it when the enable signal is low. The lowest half of the word is sent first.

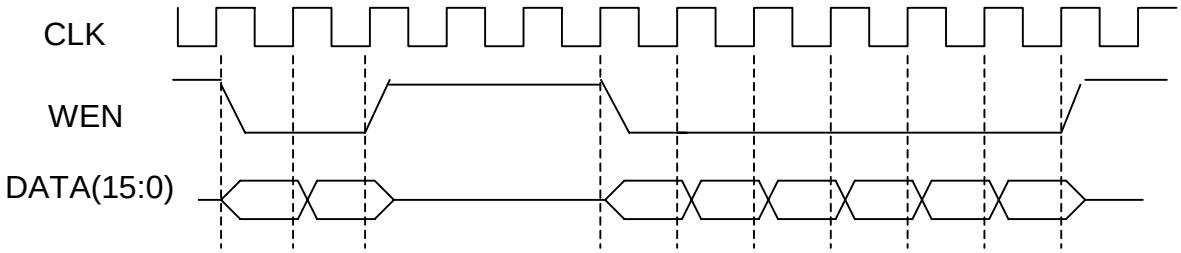



**Figure 1: Timing diagram of the data transmission**

The timing diagram is showing the transfer of a 32-bit word followed by one of three 32-bit words.

**Input and Output levels**

| Input /Output Standard | VIL | | VIH | | VOL | VOH | IOL | IOH |
|---|---|---|---|---|---|---|---|---|
| | V, min | V, max | V, min | V, max | V, max | V, min | mA | mA |
| LVTTL | -0.5 | 0.8 | 2.0 | 5.5 | 0.4 | 2.4 | 24 | -24 |

**Table 1: Voltage specifications**

VIL and VIH are recommended input voltages.

VOL and VOH are guaranteed output voltages.

IOL and IOH are guaranteed output current.

**Bus exchange**

For the bi-directional transmission 2 signals are used for the bus exchange.

The two bus-arbiters (one in each SDB interface) use the REQ, ACK signals to define which one transmits and which one receives.

- **Reset**: A receiver must be connected to a transmitter but the transmission can start in any direction.

- **Transmission**: The transmitter drives the clock, the enable and the data signals to transmit and the ack signal to reply to the bus request. The receiver drives the req signal to request a bus exchange and the ack to stop the transmssion.

- **Request**: The receiver can at any time make a request the bus. The transmitter will give the bus immediately or keep it as long as it has got data to transmit. (User controllable).

- **Exchange**: The transmitter acknowledges the request made and frees the bus. The receiver becomes the transmitter and can then use the bus.
- **Interruption**: At any time the receiver can interrupt the transmission if its reception FIFO gets full without losing data. The transmission will go on when the receiver decides it or in any case when FIFO is empty again (User controllable).

The input and output busses are independent so the transmission is possible while emptying the FIFO containing the data previously received.

A uni-directional SDB interface can use or not the bi-directional pins, which in that case provides the safety of interrupting the transmission if the FIFO of the receiver is full.

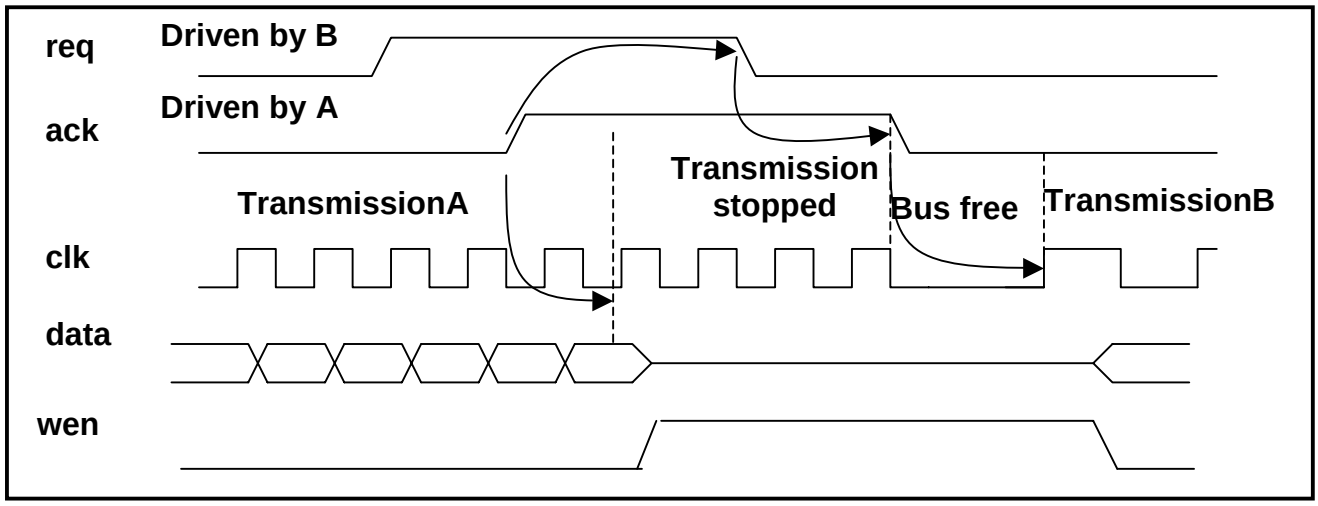



**Figure 2: Bus exchange between interfaceA and interfaceB**

B requests the bus by setting req high.

A replies by setting ack high and ends its transmission.

B replies setting req low.

A sets ack low once req is low and its transmission is finished and becomes a receiver (free the bus).

B drives the bus signals.

If the exchange is allowed and occurs in the middle of a transmission a 32-bit data (2 clock-cycles of the transmitter) will be transferred after ack is high.

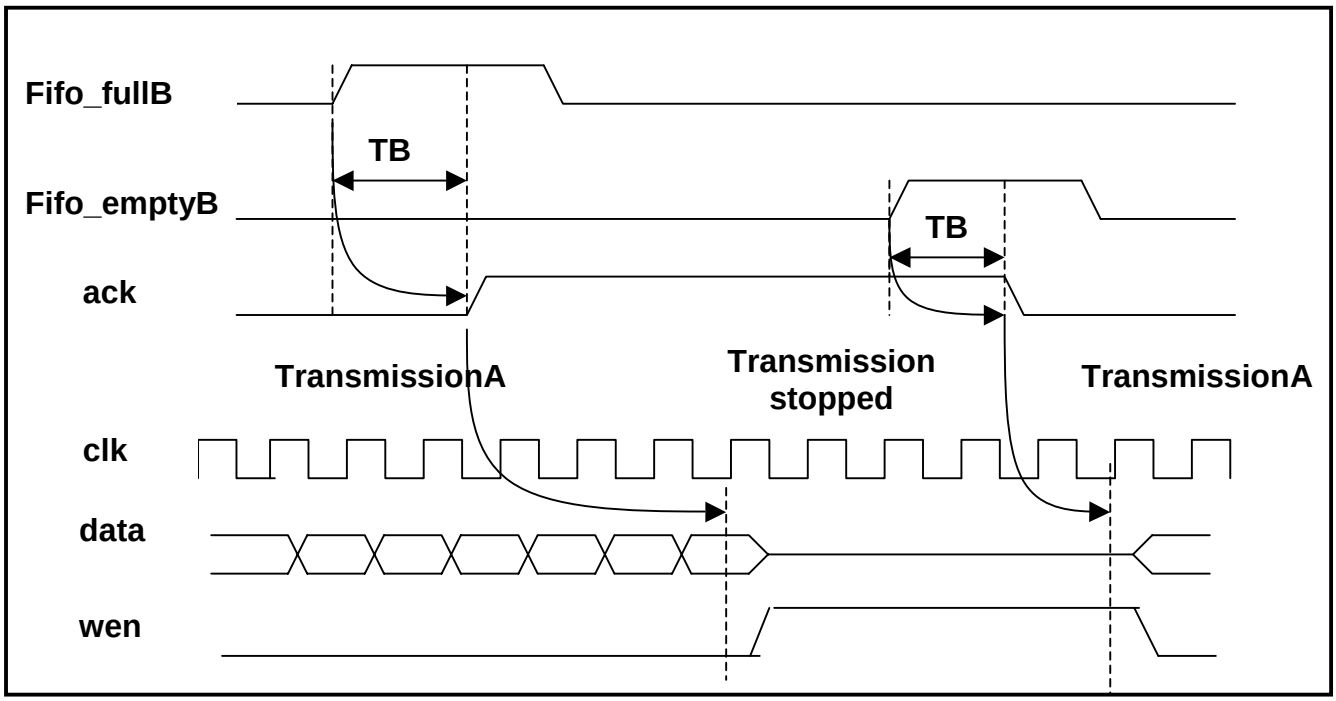



**Figure 3: Longest interruption of the transmission by interfaceB**

Once the reception FIFO is full the receiver requests the interruption of the transmission setting ack high.

The transmitter stops its transmission and waits for ack to be low to go on transmitting.

The receiver sets ack low when the FIFO is empty or when the user enables the transmission again.

Two 32-bit data are sent after ack is set high (in 4 clock cycles) but the clock frequency of B (TB is the period) defines the amount of extra data to be able to store once the FIFO is full. An extra 15x32-bit word FIFO included enables a maximum clock ratio of 20:1 between the transmission clocks on each side.

## 2. The source code

The interface for the Sundance Digital Bus has been written in VHDL.

The source code can be provided upon signing a Non-Disclosure Agreement.

The complete architecture is the following. But it can be parameterised to generate only the transmitter part, the receiver part (with or without the bus arbitration module for the interruption of the transmission) and the complete bi-directional interface.

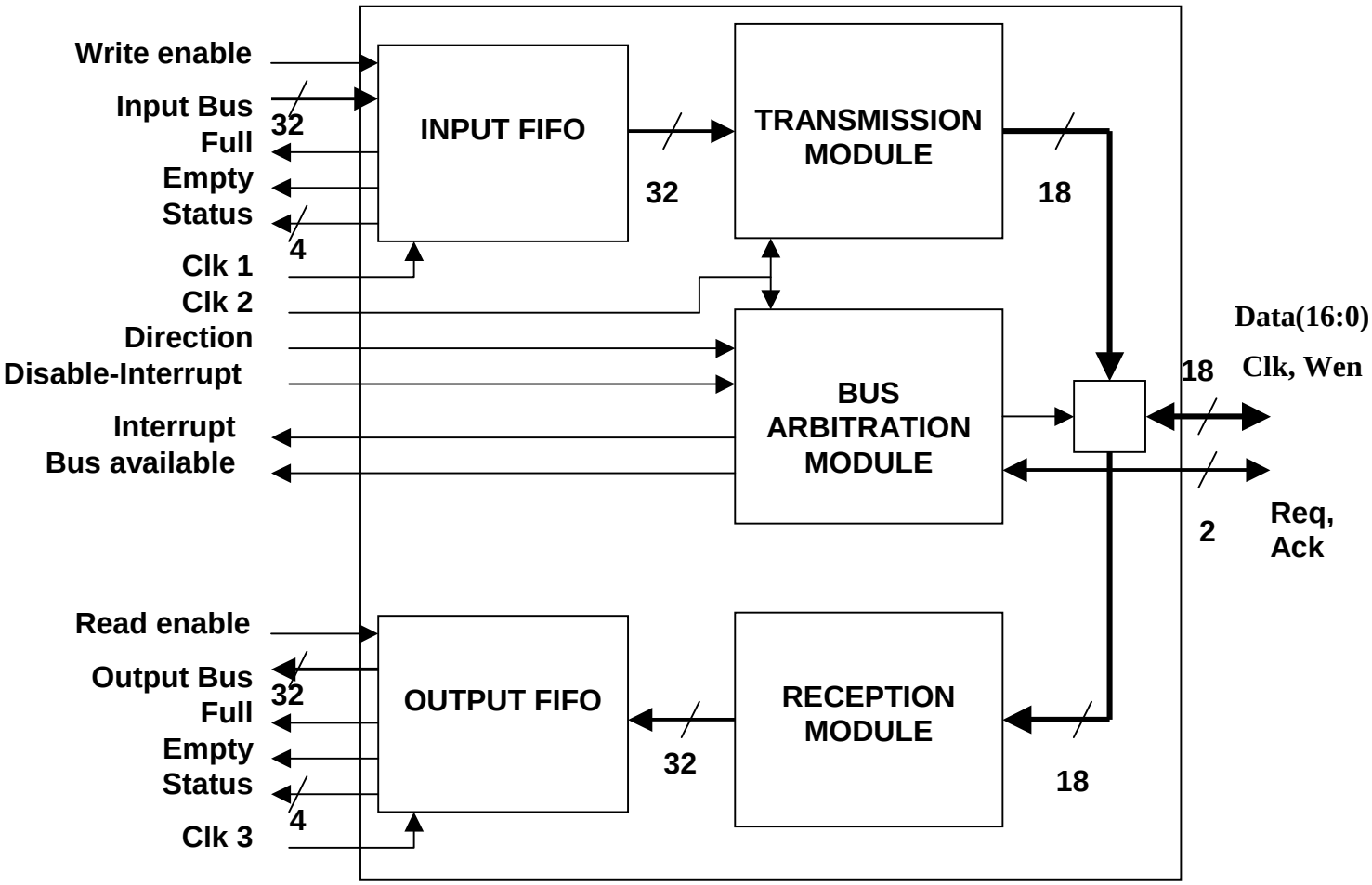



**Figure 4: Architecture of the interface**

## 3. Design performances

The interface has been tested in a Virtex Xilinx FPGA XV300-4. It uses 8% of it.

Bi-directional transmissions at 100MHz have been achieved.

The size of the design is the following

**Bi-directional interface:**

CLB: 132

* Flip-flop: 263
* Distributed block of RAM: 32

108 I/O

4 dedicated blocks of RAM.

1 Global clock buffer

Total equivalent gate count for design (including the RAM): 73,734

It is double buffered with 255x32 FIFO in input and output. An extra 15x32 FIFO is used on the reception side for the transfer interruption.

**Receiving interface:**

CLB: 72

* Flip-flop: 125
* Distributed block of RAM: 32

58 I/O

2 dedicated blocks of RAM.

1 Global clock buffer

Total equivalent gate count for design (including the RAM): 38,792

**Transmitting interface:**

CLB: 39

* Flip-flop: 99

63 I/O

2 dedicated blocks of RAM.

Total equivalent gate count for design (including the RAM): 34,304

## 4. Data Connector Pin-out

18 pins are used by a simple unidirectional interface.

20 pins are used by a bi-directional interface.

There are two spare pins that can be used for other types of synchronisation between boards.

**Pin-out**

| Function | Pin | Pin | Function |
|---|---|---|---|
| GND | 2 | 1 | **CLK** |
| GND | 4 | 3 | **D0** |
| GND | 6 | 5 | **D1** |
| GND | 8 | 7 | **D2** |
| GND | 10 | 9 | **D3** |
| GND | 12 | 11 | **D4** |
| GND | 14 | 13 | **D5** |
| GND | 16 | 15 | **D 6** |
| GND | 18 | 17 | **D7** |
| GND | 20 | 19 | **D8** |
| GND | 22 | 21 | **D9** |
| GND | 24 | 23 | **D10** |
| GND | 26 | 25 | **D11** |
| GND | 28 | 27 | **D12** |
| GND | 30 | 29 | **D13** |
| GND | 32 | 31 | **D14** |
| GND | 34 | 33 | **D15** |
| GND | 36 | 35 | **USERDEF0** |
| **REQ** | 38 | 37 | **WEN** |
| **ACK** | 40 | 39 | **USERDEF1** |

**Table 2: Data connector pin-out**

## 5. The protocol extension

The two spare pins can be used in a system as custom synchronisation lines between boards but they can be used as well to increase the transfer complexity.

Here is an example of what is possible to do:

A Sundance Digital Bus can be shared between up to four devices using these two spare pins.

At reset a transmitter would be connected to three receivers.

Each of the board would have an address. The transmitter would be able to transmit data to a specific receiver. The two user pins would be used to define the destination of the data. It would be able to send to any of the receivers and exchange the bus with any of them willing to. This receiver would then become the transmitter and send data to any of the 3 others.

This is to help you to see how the SDB can be used in a system. It is designed as a point to point transfer link but can be customised according to your system specification.

# 6. The existing standard conversion

### Low Voltage Differential Signalling (LVDS)

The SMT373 can provide a Low Voltage Differential Signalling (LVDS) extension of the SDB for long distance external connections. It can convert two sets of SDB signals (20bits) to LVDS. Each transceiver used is specified for 400Mb/s.

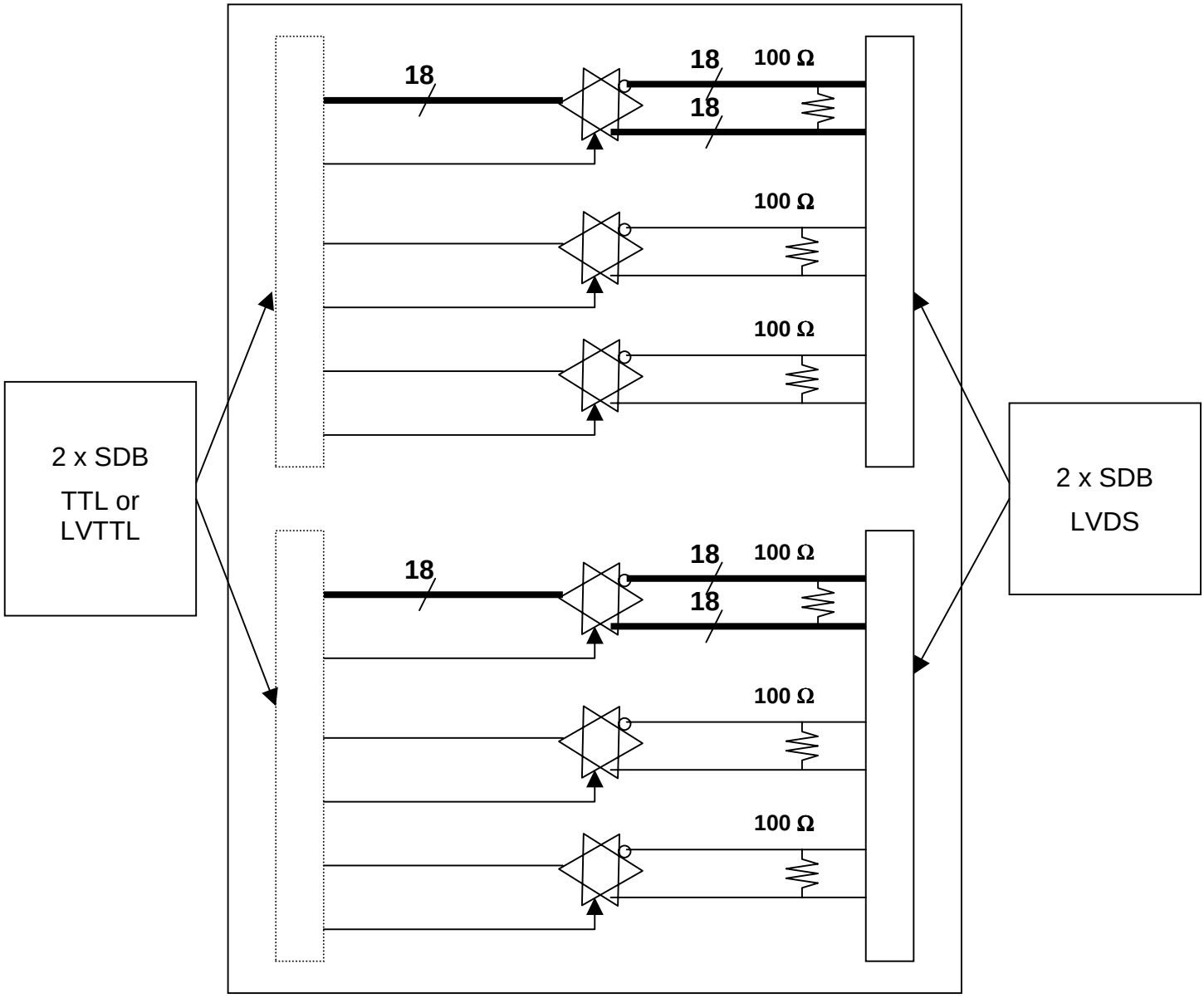
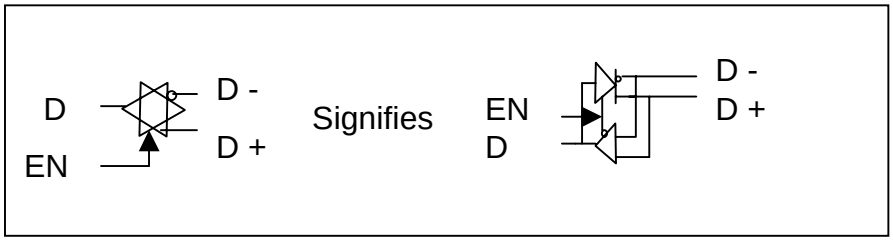



**Figure 5 Connectivity diagram**

## Legend



The pin-out needed on the SDB is the following.

| Function | Pin | Pin | Function |
|---|---|---|---|
| GND | 2 | 1 | **CLK** |
| GND | 4 | 3 | **D0** |
| GND | 6 | 5 | **D1** |
| GND | 8 | 7 | **D2** |
| GND | 10 | 9 | **D3** |
| GND | 12 | 11 | **D4** |
| GND | 14 | 13 | **D5** |
| GND | 16 | 15 | **D6** |
| GND | 18 | 17 | **D7** |
| GND | 20 | 19 | **D8** |
| GND | 22 | 21 | **D9** |
| GND | 24 | 23 | **D10** |
| GND | 26 | 25 | **D11** |
| GND | 28 | 27 | **D12** |
| GND | 30 | 29 | **D13** |
| GND | 32 | 31 | **D14** |
| GND | 34 | 33 | **D15** |
| **DIR0** | 36 | 35 | **USERDEF0** |
| **DIR2** | 38 | 37 | **WEN** |
| **DIR1** | 40 | 39 | **USERDEF1** |

**Table 3: Data connector pin-out for the LVDS extension**

DIR0 sets the direction of the line USERDEF0, DIR1 of the line USERDEF1 and DIR2 of lines D0 to D15, CLKIN and WEN. The pins USERDEF0 and USERDEF1 can be used for the bus arbitration to provide the bi-directional interface.

| Function | Pin | Pin | Function |
|---|---|---|---|
| **CLKIN +** | 2 | 1 | **CLKIN -** |
| **D0 +** | 4 | 3 | **D0 -** |
| **D1 +** | 6 | 5 | **D1 -** |
| **D2 +** | 8 | 7 | **D2 -** |
| **D3 +** | 10 | 9 | **D3 -** |
| **D4 +** | 12 | 11 | **D4 -** |
| **D5 +** | 14 | 13 | **D5 -** |
| **D6 +** | 16 | 15 | **D6 -** |
| **D7 +** | 18 | 17 | **D7 -** |
| **D8 +** | 20 | 19 | **D8 -** |
| **D9 +** | 22 | 21 | **D9 -** |
| **D10 +** | 24 | 23 | **D10 -** |
| **D11 +** | 26 | 25 | **D11 -** |
| **D12 +** | 28 | 27 | **D12 -** |
| **D13 +** | 30 | 29 | **D13 -** |
| **D14 +** | 32 | 31 | **D14 -** |
| **D15 +** | 34 | 33 | **D15 -** |
| **USERDEF0 +** | 36 | 35 | **USERDEF0 -** |
| **WEN+** | 38 | 37 | **WEN -** |
| **USERDEF1 +** | 40 | 39 | **USERDEF1 -** |

**Figure 6 LVDS connector pin-out**

Cf. SMT373 user manual for more details.

### RS485/RS422

The SMT373 can provide a RS422 or RS485 extension of the SDB according to the same pin-out as the one shown for the LVDS.

# 7. Hardware

The cables are 0.635mm pitch, 40 way.

High Density IDC (Insulation Displacement Connector) from ODU are used Part number 525.060.035.040.000.

The mating header on the board is 40-Way ODU Header Part number 515.568.035.040.000.

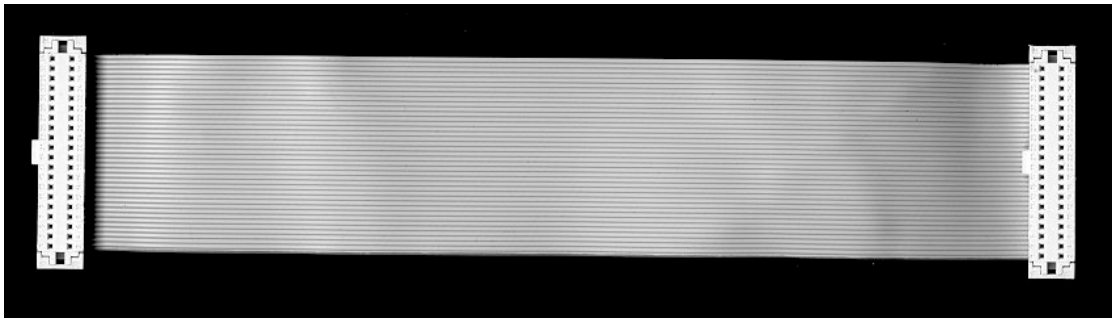


**Figure 7: SDB cables**

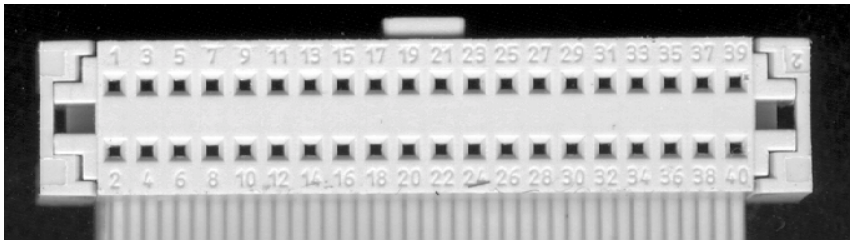



**Figure 8: Cable connector**

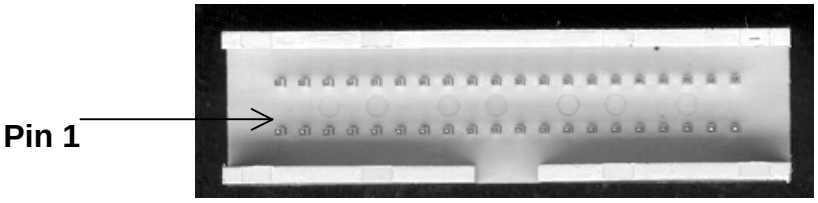



**Figure 9: Board connector Top view**

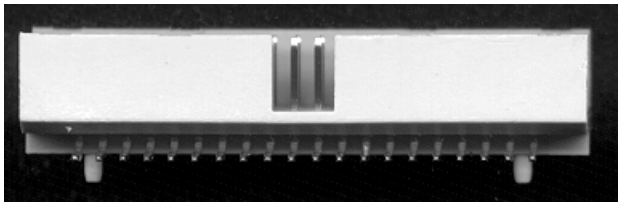


**Figure 10: Board connector Side view**